REMARKS

Claims 1, 4-5, 12, 14, 33-34, 39, 47, and 52 have been amended. Claims 2-3, 7, 10-11, 13, 19, 36-37, 40, 43-44, and 48-50 have been cancelled. No new claims have been added. Thus, claims 1, 4-6, 8-9, 12, 14-18, 20-35, 38-39, 41-42, 45-47, and 51-53 are pending.

Claims 1-7, 10-18, 20-23, and 30-51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Boehl (U.S. Patent No. 5,654,708). Claims 8-9, 24-29, and 52-53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boehl in view of Yiannoulos (U.S. Patent No. 5,982,318). These rejections are respectfully traversed.

Claim 1 recites, *inter alia*, "wherein said plurality of capacitors are used for both analog to digital conversion and for calibration, said control circuit stores in said plurality of level latches levels associated with calibration, and said plurality of level latches are connected to control a level applied to respective bottom plates of said capacitors."

Claim 16 recites, *inter alia*, "a plurality of value latches, each storing a value, and each associated with one of said plurality of capacitors, and changing a value applied to said bottom plate of said capacitor; wherein the same said capacitors are used both for calibration and for A/D conversion."

Claim 33 recites, *inter alia*, "wherein said converting uses the plurality of said first capacitors by supplying the signal to be converted to the top plates of said first capacitors while setting respective levels of said bottom plates of said first capacitors based on a respective plurality of calibration levels from said calibration."

Claim 47 recites, *inter alia*, "wherein said value stored in said latch is a multiple bit value, each bit of said multiple bit value respectively associated with, and

for controlling a level of a bottom plate of, an individual one of said plurality of capacitors."

Claim 52 recites, *inter alia*, "the same capacitors being used both for said calibration and for said conversion, and further comprising a latch, having a plurality of digital storage portions, each formed of CMOS, and each storing a value based on said calibration, said values used for setting a level of a bottom plate of said plurality of capacitors."

Boehl is directed to an analog-to-digital (A/D) converter (Fig. 1) which includes a first set of capacitors C1a, C1b, C2, ..., C8 which are utilized for both analog-to-digital conversion and for calibration of the converter, as well as conversion capacitor Ck. Referring also to Fig. 2 it can be seen that the a common line 16 is formed across the top plate each of the capacitors and supplied as an input to comparator 12. The common line can also be switchably coupled to a reference voltage (Vm). The bottom plates of the capacitors can be controlled by the control unit 11 to be coupled to either the reference voltage Vm, two other voltages (Vss, Vdd), or the input signal being converted (Vi). A RAM 34 stores a calibration value which is supplied to a digital-to-analog (D/A) converter 14, and converted into a calibration voltage Vk, which can be switchably coupled to only the calibration capacitor Ck.

The A/D conversion begins by presenting the input signal Vi to the bottom plates of each of the first set of capacitors (C1a, C1b, C2, ..., C8) while presenting the reference voltage (Vm) to the top plates of the first set of capacitors (C1a, C1b, C2, ..., C8) and the top plate of the calibration capacitor Ck. Then, a successive approximation algorithm is performed by sequencing the bottom plates of the first set of capacitors (C1a, C1b, C2, ..., C8) between voltage levels Vdd and Vss while operating the comparator 12. The calibration is applied to the conversion process by reading an

appropriate calibration value from RAM 34 and converting the value into a calibration voltage (Vk) by D/A converter 14. The calibration voltage is supplied solely to the bottom plate of the calibration capacitor Ck.

Boehl is therefore directed to an A/D converter which uses a set of capacitor for both A/D conversion and calibration, but which also applies the calibration by latching a single calibration value and applying that calibration value (as a voltage) to a single calibration capacitor. By contrast, the amended independent claims recite an apparatus or method in which a plurality of latches each storing a calibration value is used to alter the voltages of the set of capacitors used for both A/D conversion and calibration. Boehl therefore fails to teach or suggest the above recited limitations of the independent claims.

Yiannoulos is directed to a analog-to-digital converter which supports white balancing and gamma correction in imaging applications. However, Yiannoulos is cited for its teaching of MOS technology, and does not disclose or suggest the above recited limitations of the independent claims.

Claims 1, 16, 33, 57, and 52 are therefore believed to be allowable over the prior art of record. The depending claims (4, 5, 6, 8-9, 12, 14-15, 17-18, 20-32, 34-35, 41-42, 45, 49, 51, and 53) are also believed to be allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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